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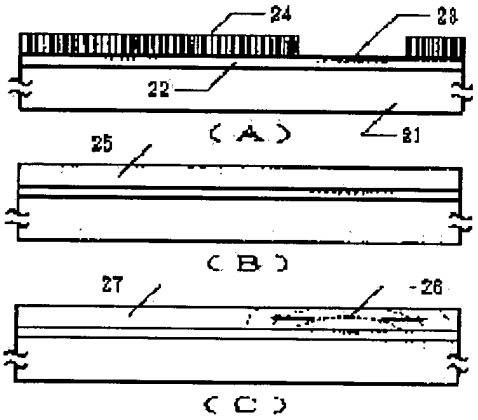
(54) SEMICONDUCTOR AND MANUFACTURE OF SEMICONDUCTOR DEVICE

(57)Abstract:
PURPOSE: To provide a method by which the crystallizing time of amorphous silicon is reduced by lowering the crystallizing temperature of the amorphous silicon and another method by which a thin film transistor is manufactured by using the method.
CONSTITUTION: After depositing a base insulating film (e.g. silicon oxide film 22), the insulating film is subjected to plasma treatment by exposing the film to a plasma atmosphere, and then, an amorphous silicon film 25 is deposited and the amorphous silicon is crystallized at 400-600°C. In addition, a part 26 having excellent crystallinity is arbitrary formed by selectively exposing the film 25 to the plasma atmosphere so as to control the part where a crystal core is produced. The semiconductor thus manufactured is used for a thin film transistor.



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* NOTICES *

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2.**** shows the word which can not be translated.
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CLAIMS

[Claim(s)]
[Claim 1] The production technique of the semiconductor characterized by having the process which forms an insulating coat in a substrate, the process which exposes the aforementioned insulating coat to a plasma, the process which forms the silicon layer of the amorphous status after the aforementioned process and on the aforementioned insulating coat, and the process which processes the aforementioned silicon layer at 400 degrees C - 600 degrees C.
[Claim 2] It is the production technique of the semiconductor characterized by the substrate being heated by 100-500 degrees C in the process exposed to a plasma in a claim 1.
[Claim 3] The plasma used in a claim 1 is the production technique of the semiconductor characterized by containing at least one, nitrogen, oxygen, neon, a krypton, or an argon, more than 10 volume %.
[Claim 4] It is the production technique of the semiconductor characterized by being carried out, without exposing a substrate to the atmospheric air between the process which exposes the insulating coat on a substrate to a plasma in a claim 1, and the process which forms the silicon layer of the amorphous status on an insulating coat.
[Claim 5] The process which exposes the insulating coat on a substrate to a plasma in a claim 1 is the production technique of the semiconductor characterized by being carried out in the space which has the electrode constituted by the material containing nickel, iron, cobalt, and at least one element of platinum.
[Claim 6] The production technique of the semiconductor characterized by to have the process which forms an insulating coat on a substrate, the process which covers the aforementioned insulating coat with mask material alternatively, the process which exposes a substrate to a plasma, the process which form the silicon layer of the amorphous status after the aforementioned process and on the aforementioned insulating coat, the process which process the aforementioned silicon layer at 400 degrees C - 600 degrees C, and the process which etch the aforementioned silicon layer alternatively.
[Claim 7] The process which forms an insulating coat on a substrate in the process which produces TFT, The process which covers the aforementioned insulating coat with mask material alternatively, and the process which exposes a substrate to a plasma, The process which forms the silicon layer of the amorphous status after the aforementioned process and on the aforementioned insulating coat, The production technique of the semiconductor device characterized by having the process which processes the aforementioned silicon layer at 400 degrees C - 600 degrees C, the process which etches the aforementioned silicon layer alternatively, and the process which makes the fraction previously covered with mask material the channel formation field of TFT.

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] The example of the equipment which carries out this invention is shown. (Example 1 reference)
[Drawing 2] The process of an example 2 is shown. (Example crystallized alternatively)
[Drawing 3] Production process drawing (cross section) of TFT by the example 3 is shown.
[Drawing 4] Production process drawing (cross section) of TFT by the example 4 is shown.
[Drawing 5] The example of the equipment which carries out this invention is shown. (Example 1 reference)
[Drawing 6] The annealing time dependency of the Raman-scattering intensity of the silicon layer obtained according to the example 1 is shown. (Relative intensity when a peak ratio sets the Raman-scattering intensity of a standard sample (single crystal silicon) to 1)
[Drawing 7] The annealing-temperature dependency of the Raman-scattering intensity of the silicon layer obtained according to the example 1 is shown. (Relative intensity when a peak ratio sets the Raman-scattering intensity of a standard sample (single crystal silicon) to 1)
[Description of Notations]
11 ... Chamber 12 ... Gas feed system
13 ... Exhaust air system 14 ... RF power
15, 16 ... Electrode 17 ... Substrate (sample)
18 ... RF plasma
21 ... Substrate 22 ... Substratum oxidization silicon layer
23 ... Field by which the plasma treatment was carried out 24 ... Mask material
25 ... Amorphous silicon layer 26 ... Crystallization silicon layer
27 ... Silicon layer which is not crystallized
30 ... Substrate 31 ... Substratum oxidization silicon layer
32 ... Mask material 33 ... Plasma
34 ... Crystalline silicon field 35 ... Gate insulator layer (oxidization silicon)
36 ... Gate electrode (N type silicon)
37 ... Impurity range (the source, drain)
38 ... Layer insulation object 39 ... A source electrode, drain electrode
40 ... Substrate 41 ... Substratum oxidization silicon layer
42 ... Plasma 43 ... Amorphous silicon field
44 ... Crystalline silicon field 45 ... Gate insulator layer (oxidization silicon)
46 ... Gate electrode (aluminum)
47 ... Anodic oxidation object (aluminum oxide)
48 ... Impurity range (the source, drain)
49 ... Layer insulation object 50 ... A source electrode, drain electrode
501 ... Spatter chamber 502 ... Electrode (sample side)
503 ... Electrode (target side) 504 ... RF power
505 ... Target 506 ... Sample (substrate)
507 ... Gas (oxygen/Ar) system 508 ... Gas (nitrogen) system
509 ... Exhaust air system 510 ... Spare room
511 ... Sample (substrate) 521 ... Plasma CVD chamber
522 ... Electrode (sample side) 523 ... Electrode (opposite side)
524 ... RF power 525 ... Sample (substrate)
526 ... Gas (silane/hydrogen) system 527 ... Exhaust air system

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[Translation done.]